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(71) Applicant: **3M INNOVATIVE PROPERTIES COMPANY** [US/US]; 3M Center, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(72) Inventors: **KELLEY, Tommie, W.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **BOARDMAN, Larry, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **DUNBAR, Timothy, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **JONES, Todd, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **MUYRES, Dawn, V.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **PELLERITE, Mark, J.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **SMITH, Terrance, P.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(74) Agents: **WEISS, Lucy, C.** et al.; Office of Intellectual Property Counsel, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

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(54) Title: ORGANIC THIN FILM TRANSISTOR WITH SILOXANE POLYMER INTERFACE

(57) Abstract: Provided is an organic thin film transistor comprising a siloxane polymeric layer interposed between a gate dielectric and an organic semiconductor layer. An integrated circuit comprising thin film transistors and methods of making a thin film transistor are also provided. The organic thin film transistors of the invention typically exhibit improvement in one or more transistor properties.

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ORGANIC THIN FILM TRANSISTOR WITH SILOXANE POLYMER INTERFACE

Technical Field

5 This invention relates to organic thin film transistors having improved performance. More particularly, the invention relates to organic thin film transistors having a siloxane polymeric layer between the semiconductor and gate dielectric and methods of making such transistors.

Background

10 Organic semiconductors are of great interest for a variety of applications involving low-cost electronics. It is believed that organics can be synthesized to incorporate the necessary electronic properties for a wide variety of devices, and also can be constructed to allow low-cost, reel-to-reel processing that is not currently possible for crystalline silicon microelectronics.

15 One area of concern in organic electronic devices is the quality of the interface formed between the organic semiconductor and another device layer. Prior work on the interface between the semiconductor and the gate dielectric has included using silazane or silane coupling agents on silicon oxide surfaces. Silane coupling agents can require complex deposition processes.

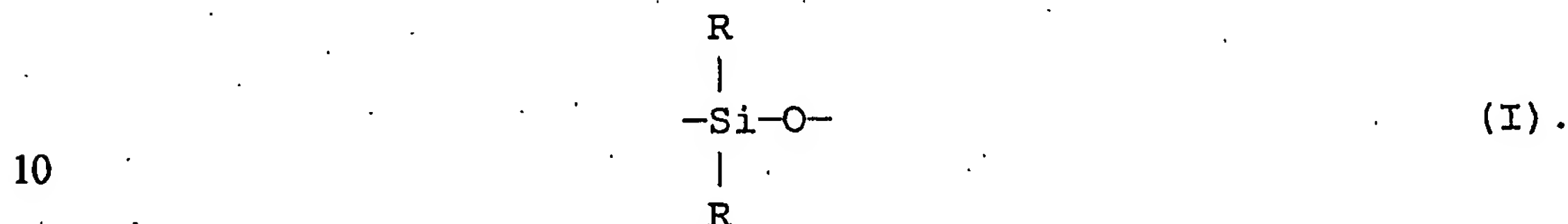
20 EP 1041652 A2 describes the use of several surface treatments to enhance the crystalline domain size of solution-cast oligothiophenes on SiO_x for thin film transistors (TFTs), although measured charge carrier mobility values were generally lower than the untreated controls. Other work involving surface treatments in TFTs involved poly(vinyl alcohol) layers, which may be relatively thick. In rare instances, previous work has shown
25 minor improvements in mobility. The predominant effects shown in the previous work have been no improvement and/or detrimental effects on mobility, without regard for other important aspects of device performance.

Summary

30 The present inventors discovered materials for and methods of improving the properties of organic thin film transistors by controlling the interface between the organic

semiconductor and the dielectric material. The organic thin film transistors of the invention also are suitable for low-cost manufacturing processes.

The present invention provides a substantially nonfluorinated polymeric layer having a thickness less than about 400Å interposed between a gate dielectric and an organic semiconductor layer in an OTFT. The polymeric layer comprises a polymer having interpolymerized units according to the formula:



In this formula, each R comprises, independently, a group selected from hydrogen, C₁-C₂₀ aliphatic, C₄-C₂₀ alicyclic, arylalkyl, or aryl, and a combination thereof which may contain one or more heteroatom(s) and/or one or more functional group(s).

In another aspect, the present invention provides a method of making an OTFT comprising providing a substrate, forming a gate electrode on the substrate, forming a gate dielectric on the gate electrode, applying a substantially nonfluorinated polymeric layer having a thickness less than about 400Å interposed between the gate dielectric and an organic semiconductor layer, depositing an organic semiconductor layer adjacent to the polymeric layer, and depositing a source electrode and a drain electrode contiguous to the organic semiconductor layer. An integrated circuit comprising OTFTs is also provided.

Any known thin film transistor construction option is possible with the invention. For example, the source and drain electrodes may be adjacent to the gate dielectric with the organic semiconductor layer over the source and drain electrodes, or the organic semiconductor layer may be interposed between the source and drain electrodes and the gate dielectric. In each option, the invention provides a siloxane polymeric layer between the organic semiconductor layer and the gate dielectric.

The present invention provides organic thin film transistors with one or more improvements over known devices. With the present invention, improvements in properties such as threshold voltage, subthreshold slope, on/off ratio, and charge-carrier mobility can be achieved. In addition, large improvements in at least one property, such as charge-carrier mobility, can be achieved with the invention, while maintaining other OTFT properties within desirable ranges. The improvements in device performance provided by the present invention enable the production by simpler processing conditions

of complex circuits having higher operating speeds than an OTFT made without the polymer layer. This invention also enables the production of larger circuit elements having comparable performance to devices with very small features. Devices with larger feature sizes can be less expensive as they do not require expensive precision patterning methods.

As used herein, "a" or "an" or "the" are used interchangeably with "at least one", to mean "one or more" of the element being modified.

Other features and advantages of the invention will be apparent from the following detailed description of the invention and the claims. The above summary of principles of the disclosure is not intended to describe each illustrated embodiment or every implementation of the present disclosure. The detailed description that follows more particularly exemplifies certain preferred embodiments utilizing the principles disclosed herein.

Detailed Description

Generally, a thin film transistor includes a gate electrode, a gate dielectric on the gate electrode, a source electrode and a drain electrode adjacent to the gate dielectric, and a semiconductor layer adjacent to the gate dielectric and adjacent to the source and drain electrodes. More specifically, an organic thin film transistor (OTFT) has an organic semiconductor layer. Such OTFTs are known in the art as shown, for example, in copending application USSN 09/947,845, Attorney Docket No. 56999US002, filed on September 6, 2001.

The organic thin film transistor of the present invention further includes a siloxane polymeric layer interposed between the gate dielectric and the organic semiconductor layer.

Substrate

A substrate can be used to support the OTFT, *e.g.*, during manufacturing, testing, storage, use, or any combination thereof. The gate electrode and/or gate dielectric may provide sufficient support for the intended use of the resultant OTFT and another substrate is not required. For example, doped silicon can function as the gate electrode and support the OTFT. In another example, one substrate may be selected for testing or screening various embodiments while another substrate is selected for commercial embodiments. In

another embodiment, a support may be detachably adhered or mechanically affixed to a substrate, such as when the support is desired for a temporary purpose. For example, a flexible polymeric substrate may be adhered to a rigid glass support, which support could be removed. In some embodiments, the substrate does not provide any necessary
5 electrical function for the OTFT. This type of substrate is termed a "non-participating substrate" in this document.

Useful substrate materials can include organic and/or inorganic materials. For example, the substrate may comprise inorganic glasses, ceramic foils, polymeric materials, filled polymeric materials, coated metallic foils, acrylics, epoxies, polyamides,
10 polycarbonates, polyimides, polyketones, poly(oxy-1,4-phenyleneoxy-1,4-phenylenecarbonyl-1,4-phenylene) (sometimes referred to as poly(ether ether ketone) or PEEK), polynorbornenes, polyphenyleneoxides, poly(ethylene naphthalenedicarboxylate) (PEN), poly(ethylene terephthalate) (PET), poly(phenylene sulfide) (PPS), and fiber-reinforced plastics (FRP).

15 A flexible substrate is used in some embodiments of the present invention. This allows for roll processing, which may be continuous, providing economy of scale and economy of manufacturing over some flat and/or rigid substrates. The flexible substrate chosen preferably is capable of wrapping around the circumference of a cylinder of less than about 50 cm diameter without distorting or breaking. The substrate chosen more
20 preferably is capable of wrapping around the circumference of a cylinder of less than about 25 cm diameter without distorting or breaking the substrate. In some embodiments, the substrate chosen most preferably is capable of wrapping around the circumference of a cylinder of less than about 10 cm diameter, or even about 5 cm diameter, without distorting or breaking the substrate. The force used to wrap the flexible substrate of the
25 invention around a particular cylinder typically is low, such as by unassisted hand, *i.e.*, without the aid of levers, machines, hydraulics, and the like. The preferred flexible substrate may be rolled upon itself.

Gate Electrode

The gate electrode can be any useful conductive material. For example, the gate
30 electrode may comprise doped silicon, or a metal, such as aluminum, chromium, copper, gold, silver, nickel, palladium, platinum, tantalum, and titanium. Conductive polymers also can be used, for example polyaniline, poly(3,4-ethylenedioxythiophene)/poly(styrene

sulfonate) (PEDOT:PSS). In addition, alloys, combinations, and multilayers of these materials may be useful.

Gate Dielectric

5 The gate dielectric is provided on the gate electrode, for example, through a deposition process. This gate dielectric electrically insulates the gate electrode under the operating conditions of the OTFT device from the balance of the device. Thus, the gate dielectric comprises an electrically insulating material. The gate dielectric should have a dielectric constant above about 2, more preferably above about 5. The dielectric constant of the gate dielectric also can be very high, for example, 80 to 100 or even higher. Useful
10 materials for the gate dielectric may comprise, for example, an organic or inorganic electrically insulating material, or combinations thereof.

The gate dielectric may comprise a polymeric material, such as polyvinylidene fluoride (PVDF), cyanocelluloses, polyimides, epoxies, etc. In some embodiments, an inorganic capping layer comprises the outer layer of an otherwise
15 polymeric gate dielectric for improved bonding to the polymeric layer and/or improved dielectric properties.

Specific examples of inorganic materials useful for the gate dielectric include strontiates, tantalates, titanates, zirconates, aluminum oxides, silicon oxides, tantalum oxides, titanium oxides, silicon nitrides, barium titanate, barium strontium titanate, barium
20 zirconate titanate, zinc selenide, and zinc sulfide. In addition, alloys, combinations, and multilayers of these can be used for the gate dielectric. Of these materials, aluminum oxides, silicon oxides, silicon nitrides, and zinc selenide are preferred.

The gate dielectric can be deposited in the OTFT as a separate layer, or formed on the gate such as by oxidizing, including anodizing, the gate material to form the gate
25 dielectric.

Source and Drain Electrodes

The source electrode and drain electrode are separated from the gate electrode by the gate dielectric, while the organic semiconductor layer can be over or under the source electrode and drain electrode. The source and drain electrodes can be any useful
30 conductive material. Useful materials include those materials described above for the gate electrode, for example, aluminum, barium, calcium, chromium, copper, gold, silver,

nickel, palladium, platinum, titanium, polyaniline, PEDOT:PSS, other conducting polymers, alloys thereof, combinations thereof, and multilayers thereof.

5 The thin film electrodes (*e.g.*, gate electrode, source electrode, and drain electrode) can be provided by any useful means such as physical vapor deposition (*e.g.*, thermal evaporation, sputtering), plating, or ink jet printing. The patterning of these electrodes can be accomplished by known methods such as shadow masking, additive photolithography, subtractive photolithography, printing, transfer printing, microcontact printing, and pattern coating.

Organic Semiconductors

10 Useful materials for the organic semiconductor layer include acenes. Particular examples include anthracene, tetracene, pentacene, and substituted pentacenes. Substituted pentacene compounds that are useful as organic semiconductors in the present invention comprise at least one substituent selected from the group consisting of electron-donating substituents (for example, alkyl, alkoxy, or thioalkoxy), halogen substituents, and combinations thereof. Useful substituted pentacenes include but are not limited to 2,9-
15 dialkylpentacenes and 2,10-dialkylpentacenes, wherein the alkyl group has from about 1 to 12 carbons; 2,10-dialkoxypentacenes; and 1,4,8,11-tetraalkoxypentacenes. Such substituted pentacenes are taught in copending applications USSN 09/966,954, Attorney Docket No. 57087US002, and USSN 09/966,961, Attorney Docket No. 57088US002, both
20 filed on September 26, 2001.

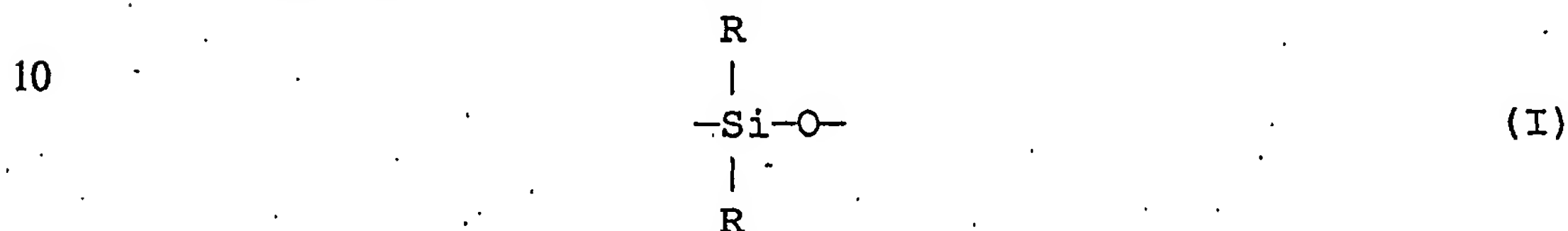
Examples of other useful organic semiconductors include perylenes, fullerenes, phthalocyanines, oligothiophenes, and substituted derivatives thereof. Particular organic semiconductor compounds include sexithiophene, α,ω -dihexylsexithiophene, quinquethiophene, quaterthiophene, α,ω -dihexylquaterthiophene, α,ω -
25 dihexylquinquethiophene, poly(3-hexylthiophene), bis(dithienothiophene), anthradithiophene, dihexylanthradithiophene, polyacetylene, polythienylenevinylene, C₆₀, copper(II) hexadecafluorophthalocyanine, and N,N'-bis(pentadecafluoroheptylmethyl)naphthalene-1,4,5,8-tetracarboxylic diimide.

30 The organic semiconductor layer can be provided by any useful means, such as for example, vapor deposition, solution deposition, spin coating, and printing techniques.

Polymeric Layer

The polymeric layer of the invention has a maximum thickness less than about 400 Angstroms (Å), more preferably less than about 200 Å, most preferably less than about 100 Å. The polymeric layer of the invention generally has a thickness of at least about 5 Å, more preferably at least about 10 Å. The thickness can be determined through known methods, *e.g.*, ellipsometry.

The polymeric layer comprises a substantially nonfluorinated polymer having interpolymerized units according to the formula:



wherein each R comprises, independently, a group selected from hydrogen, C₁-C₂₀ aliphatic, C₄-C₂₀ alicyclic, arylalkyl, or aryl, and a combination thereof which may contain one or more heteroatom(s) and/or one or more functional group(s). As used in this document, "heteroatom" means a non-carbon atom such as O, P, S, N and Si. In this document, "substantially nonfluorinated" means that less than about 5% (more preferably less than about 1% and even more preferably 0%) of the carbons in the polymeric layer have fluorine substituents.

Particular selections for R groups include, for example, methyl, phenyl, 2-phenylethyl, C₂-C₁₈ aliphatic groups, and functional group-containing moieties including, but not limited to, hydroxyl, vinyl, 5-hexenyl, hydrogen, chloro, 3-(meth)acryloxypropyl, 3-mercaptopropyl, 3-glycidoxypropyl, 2-(3,4-epoxycyclohexyl)ethyl, 3-aminopropyl, 3-acetoxypentyl, 3-chloropropyl, 3-carboxypentyl, 3-cyanopropyl, chlorophenyl, C₁-C₆ 2-(dialkylphosphono)ethyl.

Examples of useful polymeric materials include poly(dimethylsiloxane), poly(dimethylsiloxane-co-diphenylsiloxane), poly(methylphenylsiloxane-co-diphenylsiloxane), and poly(dimethylsiloxane-co-methylphenylsiloxane).

Siloxane polymers useful in the practice of this invention may be prepared by any of a number of methods familiar to those skilled in the art, including, for example, anionic, condensation, or ring-opening polymerization. Siloxane polymers useful for this invention may also be prepared with the introduction of functional end-groups or functional pendant groups. This may be accomplished through the use of functional monomers, functional

initiators, or functional chain terminators, for example, the termination of an anionically polymerized polydiorganosiloxane with a chlorotrialkoxysilane. They may also be prepared by modification of existing siloxane polymers, for example, the reaction of an olefinically functional polydiorganosiloxane with a silicon hydride, *e.g.*, trichlorosilane.

5 While this invention emphasizes the use of linear polydiorganosiloxanes in which each unit in the siloxane polymer is derived from a difunctional precursor, it is considered within the scope of this invention to employ polyorganosiloxanes that incorporate small amounts of siloxane units derived from trifunctional or tetrafunctional precursors. The number of trifunctionally- and tetrafunctionally-derived siloxane units should not exceed
10 about 10 percent, preferably about 5 percent or less, of the total average number of siloxane units in the polymer.

Useful polymeric materials may additionally include block copolymers comprising blocks of Formula (I) connected with blocks of interpolymerized units derived from an ethylenically unsaturated monomer such as styrene, butadiene, or isoprene.

15 In addition, blends of two or more polymeric or copolymeric materials may be used.

In another aspect, the OTFT of the invention incorporates a polymeric siloxane layer and has a charge carrier mobility at least 50% greater than the charge carrier mobility of a similar OTFT lacking the siloxane layer. In another aspect of the invention, the
20 OTFT has a charge carrier mobility at least $0.02 \text{ cm}^2/\text{Vs}$, preferably at least $0.10 \text{ cm}^2/\text{Vs}$, more preferably at least $1.0 \text{ cm}^2/\text{Vs}$, greater than the charge carrier mobility of a similar OTFT lacking the polymeric layer. In this document, all charge carrier mobility values are room temperature values.

The polymeric layer is provided on the gate dielectric by any known method. For
25 example, the polymeric layer can be provided through a coating process such as spray, spin, dip, knife, gravure, microcontact printing, ink jet printing, stamping, transfer printing, and vapor deposition. The polymeric layer can be provided on the gate dielectric via a solvent-based or solventless method. Presently preferred routes to the polymeric layer include solvent-based methods. When a solution of a polymeric layer precursor is
30 provided on the gate dielectric layer, the solvent is removed by a method compatible with the materials involved, for example by heating.

In one embodiment, the source and drain electrodes are deposited adjacent to the gate dielectric before providing the polymeric layer. Then, the polymeric layer is applied. After the layer comprising a polymer is complete, the organic semiconductor layer is deposited over the source and drain electrodes and over the polymeric layer adjacent to the gate dielectric. Before deposition of the semiconductor, the material deposited on the gate dielectric to provide the polymeric layer may be rinsed so the source and drain electrodes are essentially free of the polymeric layer. That is, less than about 5Å of polymeric layer, more preferably less than 1Å and most preferably no polymeric layer, is present on the source and drain electrodes.

10 OTFT Methods

The present invention also provides a method of making a thin film transistor comprising the steps of: (a) providing a substrate; (b) depositing a gate electrode material on the substrate; (c) providing a gate dielectric on the gate electrode material; (d) applying a substantially nonfluorinated polymeric layer adjacent to the gate dielectric, the polymeric layer having a thickness less than about 400Å; (e) providing an organic semiconductor layer adjacent to the polymeric layer; and (f) depositing a source electrode and a drain electrode contiguous to the organic semiconductor layer. The polymeric layer is selected from those described above, including combinations of two or more such polymeric layer materials. These steps can be performed in the order listed or in another order so long as the polymeric layer is interposed between the gate dielectric and the organic semiconductor layer. For example, the organic semiconductor layer can be provided over or under the source and drain electrodes.

Additional steps are useful in certain embodiments of the present invention. For example, rinsing may be performed after applying the polymeric layer. The polymeric layer may be applied via deposition of a polymer solution or a monomer solution which is then polymerized. The applied material may be exposed to an energy source, such as thermal radiation, UV or visible light, to remove solvent and/or crosslink the material to form the polymeric layer on the gate dielectric surface. Any combination of rinsing and/or energy-exposure may be used for particular embodiments, such as rinsing before or after heating, rinsing only, or heating without rinsing.

The present invention also provides an integrated circuit comprising a plurality of OTFTs made by the process described above and a method of making an integrated circuit

comprising providing a plurality of OTFTs of the invention. Thus, the present invention is embodied in an article that comprises one or more of the OTFTs described. Such articles include, for example, radio-frequency identification tags, backplanes for active matrix displays, smart cards, memory devices, and the like. In devices containing the OTFTs of the present invention, such OTFTs are operatively connected by means known in the art.

The entire process of making the thin film transistor or integrated circuit of the present invention can be carried out below a maximum substrate temperature of about 450°C, preferably below about 250°C. A minimum substrate temperature of about 150°C is preferred. The temperature selection generally depends on the substrate and processing parameters known in the art, once one is armed with the knowledge of the present invention contained herein. These temperatures are well below traditional integrated circuit and semiconductor processing temperatures, which enables the use of any of a variety of relatively inexpensive substrates, such as flexible polymeric substrates. Thus, the invention enables production of relatively inexpensive integrated circuits containing organic thin film transistors with significantly improved performance.

The OTFT of the present invention has one or more advantages over known organic thin film transistors. These advantages are apparent, for example, in charge-carrier mobility. The present invention provides OTFTs having a charge-carrier mobility greater than a comparison OTFT lacking the polymeric layer of the present invention. The OTFTs of the invention preferably have a charge-carrier mobility at least about 25% greater, more preferably at least about 50% greater, even more preferably at least about 75% greater, and in some embodiments at least about 100% greater, than the charge-carrier mobility of a comparison OTFT not made according to the present invention. Such improvements in charge-carrier mobility are provided while maintaining OTFT properties within desirable ranges. For example, the above-described improvements are obtained while providing a threshold voltage between about 25 and -25 V, a subthreshold slope below about 10 V/decade (absolute value), an on/off ratio of at least about 10^4 , and a charge-carrier mobility at least about 10^{-2} cm²/Vs when the semiconductor layer comprises a p-type semiconductor or at least about 10^{-4} cm²/Vs when the semiconductor layer comprises an n-type semiconductor. Various embodiments of the invention provide OTFTs with two, three, or more of these properties.

The invention provides a p-type semiconductor OTFT having a threshold voltage of between about -25 and 25 V, preferably a threshold voltage of between about 0 and -10 V, more preferably between about 0 and -5 V. The invention provides an n-type semiconductor OTFT having a threshold voltage of between about -25 and 25 V, preferably a threshold voltage of between about 10 and 0 V, more preferably between about 5 and 0 V. The invention provides an OTFT with a subthreshold slope below about 10 V/decade (absolute value), preferably a subthreshold slope below about 5 V/decade (absolute value), more preferably below about 2 V/decade (absolute value). The invention provides an OTFT with an on/off ratio of at least about 10^4 , preferably at least about 10^5 , more preferably at least about 5×10^5 , and even more preferably at least about 10^6 .

More specifically, in an embodiment having pentacene or a substituted pentacene as the organic semiconductor, the invention provides an OTFT with a charge-carrier mobility at least about $0.1 \text{ cm}^2/\text{Vs}$, more preferably at least $0.2 \text{ cm}^2/\text{Vs}$, and even more preferably at least about $0.5 \text{ cm}^2/\text{Vs}$. In some embodiments of the present invention, the charge-carrier mobility is above 1.0, or even above $2.0 \text{ cm}^2/\text{Vs}$. Particular embodiments of the present invention have shown a charge-carrier mobility greater than that reported for bulk single crystals of pentacene. In another embodiment of the invention, a pentacene OTFT has a charge-carrier mobility of at least about $2 \text{ cm}^2/\text{Vs}$, a negative threshold voltage, a subthreshold slope below about 3 V/decade, and an on/off ratio at least about 5×10^5 .

Objects and advantages of this invention are further illustrated by the following examples, but the particular materials and amounts thereof recited in these examples, as well as other conditions and details, should not be construed to unduly limit this invention.

Examples

Test Methods

A. Film Thickness

Single wavelength ellipsometry was employed to obtain estimates of polymeric layer thickness. Substrate values of Psi and Delta (ψ_s and Δ_s) were obtained from the cleaned substrates (described below) at an angle of incidence of 70° and a wavelength of 632.8 nm using a Gaertner Dual Mode Automatic Ellipsometer, model L116A

(Gaertner Co., Skokie, Illinois). The polymeric layer was applied to the substrates, and values were measured (ψ_f and Δ_f).

Ellipsometry modeling software, WVASE32 (from J. A. Woollam, Inc., Lincoln, Nebraska) was used to construct optical models appropriate to the specific polymer and substrate investigated. Material optical constants included with the program were used unless specified otherwise.

For thermal oxide on silicon substrates, the optical model consisted of 1000 Å of SiO₂ on 50 Å of an intermix layer (a Bruggeman effective medium approximation consisting of 50% SiO₂ and 50% Si) on top of a silicon substrate. The floating variables in the fit were the SiO₂ thickness, the intermix layer thickness and the intermix layer SiO₂ percentage (where the Si percentage is adjusted to make up the balance of the interlayer composition). Typical fit values were 950 – 990 Å SiO₂, 40 – 60 Å intermix consisting of 20 – 60 % SiO₂.

For alumina layers on silicon substrates, the optical model was 1500Å of Al₂O₃ on Si. The floating variables in the fit were the thickness in Angstroms (d) and refractive index (n) of the Al₂O₃. Seed values of d = 1500 and n = 1.77 were used. Typical final fit values were between 1400Å and 1700Å with n between 1.56 and 1.60.

Once the substrate parameters were determined by modeling ψ_s and Δ_s , they were fixed and a polymer layer was added to the optical model, between the air and dielectric layers. This layer had a variable thickness, but its refractive index was fixed at a value typical of that polymer in its bulk state. The refractive index of copolymer samples was estimated. The polymeric layer thickness was then varied to achieve the best fit to ψ_f and Δ_f . Each thickness reported in Table 1 (below) was the average of four measurements on each sample.

25

B. Water Contact Angle (WCA)

Static, advancing, and receding water contact angles were measured with a video contact angle apparatus (Model VCA-2500XE, from AST Products, Billerica, Massachusetts). Values reported were averages of measurements on both sides of at least three drops on each tested surface. Estimated uncertainties in these measurements were +/- 1 degree in static and advancing measurements and +/- 2 degrees in receding measurements. Surface characterization data are summarized in Table 1 (below).

C. Thin Film Transistor Performance

Transistor performance was tested at room temperature in air using techniques known in the art, for example as shown in S.M. Sze, *Physics of Semiconductor Devices*, page 442, John Wiley & Sons, New York, 1981. A Semiconductor Parameter Analyzer (model 4145A from Hewlett-Packard, Palo Alto, California) was used to obtain the results below.

The square root of the drain current (I_d) was plotted as a function of gate-source bias (V_g), from +10V to -40V for a constant source-drain bias (V_d) of -40V, and the saturation field effect mobility was calculated from the straight line portion of the curve using the specific capacitance of the gate dielectric, the channel width and the channel length. The x-axis extrapolation of this straight-line fit was taken as the threshold voltage (V_t). In addition, plotting I_d as a function of V_g yielded a curve where a straight line fit was drawn along a portion of the curve containing V_t . The inverse of the slope of this line was the subthreshold slope (S). The on-off ratio was taken as the difference between the minimum and maximum drain current (I_d) values of the I_d - V_g curve.

Substrates

Single crystal <100> orientation heavily-doped silicon wafers were obtained from Silicon Valley Microelectronics, San Jose, California. A 1500Å layer of alumina (Wafer A), or a 1000Å layer of high temperature thermal silicon oxide (Wafer B) was deposited on each wafer front via chemical vapor deposition methods. A 5000Å layer of aluminum metal was vapor deposited onto the backside of each wafer. In this demonstration, the doped wafer capped with aluminum served as the gate electrode and the aluminum oxide

or silicon oxide functioned as the gate dielectric when organic thin film transistors were prepared.

Wafer Preparation and Polymer Coating Procedure

5 Wafer substrates were quartered and cleaned by 5 min exposure in a UV/ozone chamber. The material of choice was applied by spin coating (300 rpm/5 s then 2000 rpm/15 s) a solution in toluene of the polymer named in the particular example and baked at 200°C for 30 minutes, then rinsed with toluene. Ellipsometric film thickness and water contact angles were measured using the procedures outlined above.

Semiconductor Coating Procedure

10 Pentacene (available from Aldrich Chemical) was purified in a 3-zone furnace (Thermolyne 79500 tube furnace, from Barnstead Thermolyne, Dubuque, Iowa) at reduced pressure under a constant flow of nitrogen gas.

15 The purified pentacene was deposited by sublimation under vacuum (approximately 10^{-6} Torr (or 1.33×10^{-4} Pa)) onto the polymeric surface at a rate of 0.5 Å per second to reach thickness of 500 Å as measured by a quartz crystal microbalance. Palladium or gold source and drain electrodes were then shadow masked onto the pentacene layer. The device dimensions were 40 μm to 60 μm channel length x 1000 μm channel width.

Final Steps for Device Preparation and Testing

20 Multiple OTFTs were prepared and a representative sample of at least six OTFTs was tested for each of at least two deposition runs. The averaged results appear below in Table 2.

Examples 1-2

25 Wafers were quartered and solvent cleaned and then further cleaned using the procedure described above. Poly(dimethylsiloxane) (50 cSt viscosity, available as Dow Corning 200® fluid from Dow Corning, Midland, MI) was dissolved in toluene to reach a 1.0 wt% solution, which was applied to samples of Wafer A (Example 1) and Wafer B
30 (Example 2). The solutions were applied via the Polymer Coating Procedure. Pentacene

was applied as described above. OTFTs were prepared and tested as described above. Results are shown in Tables 1 and 2 below.

Example 3

5 Poly(dimethylsiloxane-co-diphenylsiloxane) (5% diphenylsiloxane, CR524B, from General Electric Silicones, Waterford, NY) was dissolved in toluene to make a 0.15 wt% solution. This solution was applied via the Polymer Coating Procedure described above onto Wafer A samples. Pentacene was applied as described above. OTFTs were prepared and tested as described above. Results are shown in Tables 1 and 2 below.

10

Example 4

Poly(dimethylsiloxane-co-methylphenylsiloxane) (viscosity 50 cSt, available as Dow Corning 510®) was dissolved in toluene to form a 1.0 wt% solution and applied via the Polymer Coating Procedure described above onto Wafer B samples. Pentacene was applied as described above. OTFTs were prepared and tested as described above. Results are shown in Tables 1 and 2 below.

15

Comparative Examples 1-2 (CE1 and CE2)

Wafers were quartered and cleaned immediately before use using consecutive rinses in acetone, methanol, 2-propanol and water, baked on a hot plate at 100°C for 3 minutes and exposed to UV/ozone in a home built chamber for 15 minutes. Wafer A was used for CE1, and Wafer B was used for CE2. Pentacene was applied as described above. OTFTs were prepared and tested as described above. Results are shown in Tables 1 and 2 below.

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Table 1: Thickness and Water Contact Angles (WCA)

Ex.	Thickness (Å)	Advancing WCA	Static WCA	Receding WCA
1	10	106	97	66
2	13	92	87	62
3	26	112	105	96
4	13	91	84	63
CE1	N/A	<20	<20	<20
CE2	N/A	<20	<20	<20

Table 2: OTFT Performance

Ex.	Mobility (cm ² /Vs)	Threshold Voltage (V)	Sub-threshold Slope (V/decade)	On / Off Ratio
1	2.2	-1.1	1.3	4.6 x 10 ⁶
2	1.5	-4.4	1.8	2.2 x 10 ⁶
3	1.1	-1.5	1.5	2.5 x 10 ⁷
4	1.9	-5.7	1.2	2.4 x 10 ⁷
CE1	0.98	-6.7	1.7	1.9 x 10 ⁷
CE2	0.30	-8.5	4.1	1.7 x 10 ⁵

- 5 Various modifications and alterations of this invention will be apparent to those skilled in the art in view of the foregoing description, without departing from the scope and principles of this invention. Accordingly, it should be understood that this invention is not to be unduly limited to the illustrative embodiments set forth hereinabove.

We claim:

1. An organic thin film transistor (OTFT) comprising a substantially nonfluorinated polymeric layer having a thickness less than about 400Å interposed between a gate dielectric and an organic semiconductor layer, wherein the polymeric layer comprises a polymer having interpolymerized units according to the formula:



wherein each R comprises, independently, a group selected from hydrogen, C₁-C₂₀ aliphatic, C₄-C₂₀ alicyclic, arylalkyl, or aryl, and a combination thereof which may contain one or more heteroatom(s) and/or one or more functional group(s).

2. The transistor of claim 1 wherein the polymeric layer comprises poly(dimethylsiloxane), poly(dimethylsiloxane-co-diphenylsiloxane), poly(methylphenylsiloxane-co-diphenylsiloxane), or poly(dimethylsiloxane-co-methylphenylsiloxane).

3. The transistor of claim 1 wherein the polymeric layer further comprises blocks of interpolymerized units derived from an ethylenically unsaturated monomer.

4. The transistor of claim 1 wherein R comprises a group selected from methyl, vinyl, 5-hexenyl, phenyl, 2-phenylethyl, 3-(meth)acryloxypropyl, 3-mercaptopropyl, 3-glycidoxypropyl, 2-(3,4-epoxycyclohexyl)ethyl, 3-aminopropyl, 3-acetoxypentyl, 3-chloropropyl, 3-carboxypentyl, 3-cyanopropyl, and 2-(diethylphosphono)ethyl.

5. The transistor of claim 1 having at least one property selected from

- a) a threshold voltage between about -25 and 25 volts;
- b) a subthreshold slope below about 10 volts per decade (absolute value);
- c) an on/off ratio of at least about 10⁴;
- d) a charge-carrier mobility at least about 10⁻² cm²/Vs when the semiconductor layer comprises a p-type semiconductor;

- e) a charge-carrier mobility at least about 10^{-4} cm²/Vs when the semiconductor layer comprises an n-type semiconductor;
- f) a charge-carrier mobility at least about 50% greater than a comparison OTFT that lacks the polymeric layer;
- 5 g) a charge-carrier mobility at least about 0.02 cm²/Vs greater than a comparison OTFT that lacks the polymeric layer;
- h) a charge-carrier mobility at least about 0.10 cm²/Vs greater than a comparison OTFT that lacks the polymeric layer; and
- 10 i) a charge-carrier mobility at least about 1.0 cm²/Vs greater than a comparison OTFT that lacks the polymeric layer.
6. The transistor of claim 1 comprising a gate dielectric that comprises an organic electrically insulating material, optionally capped with an inorganic electrically insulating material.
- 15 7. The transistor of claim 1 comprising a gate dielectric that comprises an inorganic electrically insulating material selected from strontiates, tantalates, titanates, zirconates, aluminum oxides, silicon oxides, tantalum oxides, titanium oxides, silicon nitrides, barium titanate, barium strontium titanate, barium zirconate titanate, zinc selenide, zinc sulfide, and alloys, combinations, and multilayers thereof.
- 20 8. The transistor of claim 1 further comprising a non-participating substrate.
9. The transistor of claim 1 comprising gate, source, and drain electrodes, each independently comprising a material selected from doped silicon, metal, a conducting polymer, and combinations thereof.
- 25 10. The transistor of claim 1 wherein the organic semiconductor layer comprises a material selected from acenes, perylenes, fullerenes, phthalocyanines, and oligothiophenes.
- 30

11. The transistor of claim 1 wherein the organic semiconductor layer comprises a vapor-deposited organic semiconductor.

12. The transistor of claim 1 wherein the organic semiconductor layer comprises anthracene, tetracene, pentacene, a substituted pentacene, copper(II) hexadecafluorophthalocyanine, or sexithiophene.

13. An integrated circuit comprising a multiplicity of the transistors according to claim 1.

10

14. A method of making an organic thin film transistor comprising:

- a) providing a substrate;
- b) depositing a gate electrode material on the substrate;
- c) depositing a gate dielectric on the gate electrode material;
- d) applying a substantially nonfluorinated siloxane polymeric layer having a thickness less than about 400Å interposed between a gate dielectric and an organic semiconductor layer, wherein the polymeric layer comprises a polymer having interpolymersized units according to the formula:

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wherein each R comprises, independently, a group selected from hydrogen, C₁-C₂₀ aliphatic, C₄-C₂₀ alicyclic, arylalkyl, or aryl, and a combination thereof which may contain one or more heteroatom(s) and/or one or more functional group(s);

- e) depositing an organic semiconductor layer adjacent to the polymeric layer; and
- f) providing a source electrode and a drain electrode contiguous to the organic semiconductor layer.

30

15. The method of claim 14 wherein the steps are performed in the order listed.

16. The method of claim 14 further comprising rinsing the layered material of step (d), before or after optionally exposing the material to an energy source.

17. The method of claim 14 wherein the step of providing a polymeric layer
5 involves a coating process selected from spray, spin, dip, knife, gravure, microcontact printing, ink jet printing, stamping, transfer printing, and vapor deposition.

18. The method of claim 14 wherein the source and drain electrodes are
10 provided adjacent to the gate dielectric before the step of providing a polymeric layer on the gate dielectric.

19. The method of claim 14 further comprising rinsing the siloxane polymeric layer from any surface other than the dielectric material.

15 20. The method of claim 14 wherein the substrate is flexible.

21. The method of claim 14 carried out in its entirety below a peak substrate temperature of 250°C.

20 22. The method of claim 14 carried out on a web.

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(71) Applicant: **3M INNOVATIVE PROPERTIES COMPANY** [US/US]; 3M Center, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(72) Inventors: **KELLEY, Tommie, W.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **BOARDMAN, Larry, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **DUNBAR, Timothy, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **JONES, Todd, D.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **MUYRES, Dawn, V.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **PELLERITE, Mark, J.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US). **SMITH, Terrance, P.**; Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(74) Agents: **WEISS, Lucy, C.** et al.; Office of Intellectual Property Counsel, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

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Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*
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(54) Title: ORGANIC THIN FILM TRANSISTOR WITH SILOXANE POLYMER INTERFACE

(57) Abstract: Provided is an organic thin film transistor comprising a siloxane polymeric layer interposed between a gate dielectric and an organic semiconductor layer. An integrated circuit comprising thin film transistors and methods of making a thin film transistor are also provided. The organic thin film transistors of the invention typically exhibit improvement in one or more transistor properties.

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 5 892 244 A (DOI SYUJI ET AL) 6 April 1999 (1999-04-06) column 2 -column 3; claim 1; figures 1,3 column 5, line 19 - line 32	1,13,14 2-12, 15-22
Y A	US 6 060 333 A (DOI SYUJI ET AL) 9 May 2000 (2000-05-09) column 2, line 10 - line 28 column 2, line 34 - line 36; figure 16 column 5, line 57 -column 6, line 5 -/--	1,13,14 2-12, 15-22

☒ Further documents are listed in the continuation of box C.

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Name and mailing address of the ISA

European Patent Office, P.B. 5816 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Paisdor, B

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 786 820 A (MOTOROLA INC) 30 July 1997 (1997-07-30) column 3, line 28 - line 50; claim 1; figure 2	1,13,14
A	---	2-12, 15-22
Y	EP 0 226 208 A (SUMITOMO CHEMICAL CO) 24 June 1987 (1987-06-24) page 1, line 1 - line 37; claim 1; example 1	1,13,14
Y	--- PATENT ABSTRACTS OF JAPAN vol. 1997, no. 06, 30 June 1997 (1997-06-30) & JP 09 040779 A (TOSHIBA CORP), 10 February 1997 (1997-02-10) abstract	1,13,14
Y	--- YONG SUK YANG ET AL: "DEEP-LEVEL DEFECT CHARACTERISTICS IN PENTACENE ORGANIC THIN FILMS" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS, NEW YORK, US, vol. 80, no. 9, 4 March 2002 (2002-03-04), pages 1595-1597, XP001108417 ISSN: 0003-6951 page 1595, column 1, last paragraph -page 1596, column 2	1,13,14
Y	--- EP 1 041 652 A (LUCENT TECHNOLOGIES INC) 4 October 2000 (2000-10-04) cited in the application page 6 -page 7; figure 1; examples; table II	1,13,14
Y	--- DIMITRAKOPOULOS C D ET AL: "ORGANIC THIN-FILM TRANSISTORS: A REVIEW OF RECENT ADVANCES" IBM JOURNAL OF RESEARCH AND DEVELOPMENT, IBM CORPORATION, ARMONK, US, vol. 45, no. 1, 1 January 2001 (2001-01-01), pages 11-27, XP001150345 ISSN: 0018-8646 page 17 -page 20; figures 2A,2B,8	1,13,14
A	page 24, column 2 -----	2-12, 15-22

INTERNATIONAL SEARCH REPORT

Internat	Application No
PCT/US	02/33999

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5892244	A	06-04-1999	US 6060338 A	09-05-2000
			US 6060333 A	09-05-2000
			WO 9008402 A1	26-07-1990
			JP 2609366 B2	14-05-1997
US 6060333	A	09-05-2000	US 5892244 A	06-04-1999
			WO 9008402 A1	26-07-1990
			JP 2609366 B2	14-05-1997
			US 6060338 A	09-05-2000
EP 0786820	A	30-07-1997	US 6326640 B1	04-12-2001
			EP 0786820 A2	30-07-1997
			JP 9232589 A	05-09-1997
EP 0226208	A	24-06-1987	CA 1281840 A1	19-03-1991
			DE 3682573 D1	02-01-1992
			EP 0226208 A2	24-06-1987
			JP 7091509 B	04-10-1995
			JP 62230828 A	09-10-1987
			KR 9508002 B1	24-07-1995
			MX 169135 B	23-06-1993
JP 09040779	A	10-02-1997	NONE	
EP 1041652	A	04-10-2000	US 6265243 B1	24-07-2001
			EP 1041652 A2	04-10-2000
			JP 2000307172 A	02-11-2000
			US 2001029103 A1	11-10-2001